Abstract of the Disclosure

Disclosed is a method for reducing poly-depletion in a dual gate CMOS fabrication process. The method reduces the poly-depletion in a dual gate CMOS fabrication process by increasing the doping efficiency in a gate polysilicon film. In order to increase the doping efficiency, the method employs the following four technical principles. First, the doping efficiency is increased when the dose of N+ ion implantation is increased. Second, the doping efficiency is increased when the thickness of N+ polysilicon is reduced. Third, the increase of depletion caused by the reduction of the channel width is inhibited when the EFH is adjusted to be less than 0. Fourth, the overall doping efficiency is increased when each step of polysilicon deposition and ion implantation is divided into multiple steps.